Schilling et al. "Texram: A smart memory for texturing", IEEE Computer
Graphics and Applications, 5/96, pp. 32-41.
ART-UNIT: 261
PRIMARY-EXAMINER: Tung; Kee M.
ATTY-AGENT-FIRM: Flehr Hohbach Test Albritton & Herbert LLP
ABSTRACT:

A deferred graphics pipeline processor comprising a texture unit and a
texture memory associated with the texture unit. The texture unit applies
texture maps stored in the texture memory, to pixel fragments. The textures
are MIP-mapped and comprise a series of texture maps at different levels of
detail, each map representing the appearance of the texture at a given distance
from an eye point. The texture unit performs tri-linear interpolation from the
texture maps to produce a texture value for a given pixel fragment that
approximates the correct level of detail. The texture memory has texture data
stored and accessed in a manner which reduces memory access conflicts and thus
improves throughput of said texture unit.

39 Claims, 17 Drawing figures

---------- KWIC ---------

DEPR:
FIG. 13a is a block diagram depicting one embodiment of Read Miss Control
Circuitry 2600. Read Miss Control Circuitry 2600 receives a read

4970636	November 1990	Snodgrass et al.	364/518
5083287	January 1992	Obata et al.	395/126
5402532	March 1995	Epstein et al.	395/122
5574836	November 1996	Broemmelsiek	345/427
5684939	November 1997	Foran et al.	395/131
5710876	January 1998	Peercy et al.	395/126
5767859	June 1998	Rossin et al.	345/434
5828378	October 1998	Shiraishi	345/422
5854631	December 1998	Akeley et al.	345/419
5864342	January 1999	Kajiya et al.	345/418
5880736	March 1999	Peercy et al.	345/426
5920326	July 1999	Rentschler et al.	345/503
5949424	September 1999	Cabral et al.	345/426
5977977	November 1999	Kajiya et al.	345/418
5990904	November 1999	Griffin	345/435
6002410	December 1999	Battle	345/513
6167486	December 2000	Lee et al.	711/120

OTHER PUBLICATIONS

**Watt, "3D Computer Graphics" (2nd ed.), Chapter 4, Reflection and
Illumination Models, p. 89-126.**

**Foley et al., Computer Graphics--Principles and Practice (2nd ed. 1996),
Chapter 16, Illumination and Shading, pp. 721-814.**

**Lathrop, "The Way Computer Graphics Works" (1997) Chapter 7, Rendering
(Converting A Scene to Pixels), pp. 93-150.**

**Peercy et al., "Efficient Bump Mapping Hardware" (Computer Graphics
Proceedings, Annual Conference Series, 1997) pp. 303-306.**

	Type	Hits	Search Text	DBs
1	BRS	60	((order or ordering) with (address or addressing)).ti.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB
2	BRS	425	(jack and lane).xa. or (jack and lane).xp.	USPAT
3	BRS	1	(((order or ordering) with (address or addressing)).ti.) and ((jack and lane).xa. or (jack and lane).xp.)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB
4	BRS	10433	((order or ordering) with (address or addressing)).ab.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB
5	BRS	36	(((order or ordering) with (address or addressing)).ab.) and (((order or ordering) with (address or addressing)).ti.)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB
6	BRS	18	(((order or ordering) with (address or addressing)).ab.) and ((jack and lane).xa. or (jack and lane).xp.)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB
7	BRS	8	(out with (order or ordering) with (address or addressing)).ti.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB
8	BRS	0	("same" with (order or ordering) with (address or addressing)).ti.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB
9	BRS	1	(((out or "same") with (order or ordering) with (address or addressing)).ti.) and ((jack and lane).xa. or (jack and lane).xp.)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB
10	BRS	8	((out or "same") with (order or ordering) with (address or addressing)).ti.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB
11	BRS	2121	((out or "same") with (order or ordering) with (address or addressing)).ab.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB

	Time Stamp
1	2002/05/14 11:13
2	2002/05/14 11:11
3	2002/05/14 11:11
4	2002/05/14 11:12
5	2002/05/14 11:12
6	2002/05/14 11:13
7	2002/05/14 11:14
8	2002/05/14 11:15
9	2002/05/14 11:17
10	2002/05/14 13:26
11	2002/05/14 13:47

	Type	Hits	Search Text	DBs
12	BRS	5	(((out or "same") with (order or ordering) with (address or addressing)).ab.) and ((jack and lane).xa. or (jack and lane).xp.)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB
13	BRS	63014	365/$.ccls. or 711/$.ccls.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB
14	BRS	143	(((out or "same") with (order or ordering) with (address or addressing)).ab.) and (365/$.ccls. or 711/$.ccls.)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB
15	BRS	51030	365/$.ccls.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB
16	BRS	99	365/$.ccls. and (((out or "same") with (order or ordering) with (address or addressing)).ab.)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB
17	BRS	104317	(read or reading) with (buffer or buffering or register)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB
18	BRS	2353	((out or "same" or different) with (order or ordering) with (address or addressing)).ab.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB
19	BRS	319	(((out or "same" or different) with (order or ordering) with (address or addressing)).ab.) same ((read or reading) with (buffer or buffering or register))	USPAT; US-PGPUB; EPO; JPO; IBM_TDB
20	BRS	460	(((out or "same" or different) with (order or ordering) with (address or addressing)).ab.) and ((read or reading) with (buffer or buffering or register))	USPAT; US-PGPUB; EPO; JPO; IBM_TDB
21	BRS	39	365/$.ccls. and ((((out or "same" or different) with (order or ordering) with (address or addressing)).ab.) and ((read or reading) with (buffer or buffering or register)))	USPAT; US-PGPUB; EPO; JPO; IBM_TDB

	Time Stamp
12	2002/05/14 13:38
13	2002/05/14 13:38
14	2002/05/14 13:45
15	2002/05/14 13:45
16	2002/05/14 13:46
17	2002/05/15 14:35
18	2002/05/14 15:38
19	2002/05/14 13:49
20	2002/05/14 13:49
21	2002/05/14 15:28

	Type	Hits	Search Text	DBs
22	BRS	13316	711/$.ccls.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB
23	BRS	38	((((out or "same" or different) with (order or ordering) with (address or addressing)).ab.) and ((read or reading) with (buffer or buffering or register))) and 711/$.ccls.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB
24	BRS	65662	(order or ordering or sequence) with (address or addressing)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB
25	BRS	8534	((order or ordering or sequence) with (address or addressing)) same (read or reading) same (buffer or buffering or register)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB
26	BRS	3234	((order or ordering or sequence) with (address or addressing)) with (read or reading) with (buffer or buffering or register)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB
27	BRS	2176	(((order or ordering or sequence) with (address or addressing)) with (read or reading) with (buffer or buffering or register)) with (different or order or "not")	USPAT; US-PGPUB; EPO; JPO; IBM_TDB
28	BRS	238	((((order or ordering or sequence) with (address or addressing)) with (read or reading) with (buffer or buffering or register)) with (different or order or "not")) and 365/$.ccls.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB
29	BRS	460	(((order or ordering or sequence) with (address or addressing)) with (read or reading) with (buffer or buffering or register)) with (different or order or "not").ab.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB

	Time Stamp
22	2002/05/14 15:28
23	2002/05/14 15:28
24	2002/05/15 14:20
25	2002/05/14 15:41
26	2002/05/14 15:42
27	2002/05/14 15:44
28	2002/05/14 15:44
29	2002/05/14 15:45

	Type	Hits	Search Text	DBs
30	BRS	23	((((order or ordering or sequence) with (address or addressing)) with (read or reading) with (buffer or buffering or register)) with (different or order or "not").ab.) and 365/$.ccls.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB
31	BRS	16	((((order or ordering or sequence) with (address or addressing)) with (read or reading) with (buffer or buffering or register)) with (different or order or "not").ab.) and 711/$.ccls.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB
32	BRS	18654	(stream or streaming) with (memory or storage)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB
33	BRS	65662	(order or ordering or sequence) with (address or addressing)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB
34	BRS	3612	((order or ordering or sequence) with (address or addressing)) and ((stream or streaming) with (memory or storage))	USPAT; US-PGPUB; EPO; JPO; IBM_TDB
35	BRS	430	((order or ordering or sequence) with (address or addressing)) same ((stream or streaming) with (memory or storage))	USPAT; US-PGPUB; EPO; JPO; IBM_TDB
36	BRS	232	((order or ordering or sequence) with (address or addressing)) with ((stream or streaming) with (memory or storage))	USPAT; US-PGPUB; EPO; JPO; IBM_TDB
37	BRS	104317	(read or reading) with (buffer or buffering or register)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB
38	BRS	19	(((order or ordering or sequence) with (address or addressing)) with ((stream or streaming) with (memory or storage))) with ((read or reading) with (buffer or buffering or register))	USPAT; US-PGPUB; EPO; JPO; IBM_TDB

	Time Stamp
30	2002/05/14 16:10
31	2002/05/15 13:00
32	2002/05/15 13:58
33	2002/05/15 14:24
34	2002/05/15 14:25
35	2002/05/15 14:25
36	2002/05/15 14:25
37	2002/05/15 14:37
38	2002/05/15 14:59

	Type	Hits	Search Text	DBs
39	BRS	57013	address$ adj4 (buffer or buffering or register)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB

	Time Stamp
39	2002/05/17 11:06

miss request
from the miss logic shown in FIG. 2, when the tag mechanism determines that the
desired information is not contained in texel prefetch buffer 1216. There are
four types of read miss requests: texture look-up (miss), copy texture, read
texture, and Auxring read dualoct (a maintenance utility function). The read
miss requests received by read control circuitry 2600 are prioritized by
prioritization block 2620, for example, in the order listed above. Prioritization block 2620 sends the read request to the appropriate channel
based upon the channel bit (FIG. 8) contained in the texture memory address to
be accessed. These addresses are thus sent to request queues 2621-0 and
2621-1, which, in one embodiment, are 32 addresses deep. The addresses stored
in request queues 2621-0 and 2621-1 are applied to reorder logic circuitry
2623-0 and 2623-1, respectively, which in turn access RAMBus memory controller
2649. Reorder logic 2623-0 and 2623-1 reorder the addresses received from
request queues 2621-0 and 2621-1 in order to avoid memory conflict in texture
memory, as will be described with respect to FIG. 13b. Since reorder logic
2623-0 and 2326-1 reorder the memory addresses to be accessed by RAMBus memory
controller 2649, tag queue 2622 keeps track of channel and requester
information. The accessed data is output to in-order return queue 2624, where

the results are placed in the appropriate slots based upon the original order as indicated by queues 2609 and 2610. The data, once stored in proper order in in-order return queue 2624 is then provided to its requestor as data and a data valid signal. In one embodiment, the data is output in a 144 bits wide, which corresponds to a dualoct.

US-PAT-NO: 6288730
DOCUMENT-IDENTIFIER: US 6288730 B1
TITLE: Method and apparatus for generating texture
DATE-ISSUED: September 11, 2001
INVENTOR-INFORMATION:

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Hong; Bo	San Jose	CA	N/A	N/A
Mammen; Abraham	Pleasanton	CA	N/A	N/A

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APPL-NO: 9/ 378408
DATE FILED: August 20, 1999
PARENT-CASE:
RELATED APPLICATIONS This application claims the benefit of U.S. Provisional
Application Ser. No. 60/097,336 entitled Graphics Processor with Deferred
Shading filed Aug. 20, 1998 is hereby incorporated by reference. This
application is also related to the following U.S. patent applications, each of
which are incorporated herein by reference: Ser. No. 09/213,990, filed Dec.
17, 1998, entitled HOW TO DO TANGENT SPACE LIGHTING IN A DEFERRED SHADING
ARCHITECTURE; Ser. No. 09/378,598, filed Aug. 20, 1999, entitled APPARATUS

AND METHOD FOR PERFORMING SETUP OPERATIONS IN A 3-D GRAPHICS PIPELINE USING
UNIFIED PRIMITIVE DESCRIPTORS; Ser. No. 09/378,633, filed Aug. 20, 1999
entitled SYSTEM, APPARATUS AND METHOD FOR SPATIALLY SORTING IMAGE DATA IN A
THREE-DIMENSIONAL GRAPHICS PIPELINE; Ser. No. 09/378,439 filed Aug. 20, 1999,
entitled GRAPHICS PROCESSOR WITH PIPELINE STATE STORAGE AND RETRIEVAL; Ser.
No. 09/378,408, filed Aug. 20, 1999, entitled METHOD AND APPARATUS FOR
GENERATING TEXTURE; Ser. No. 09/379,144, filed Aug. 20, 1999 entitled
APPARATUS AND METHOD FOR GEOMETRY OPERATIONS IN A 3D GRAPHICS PIPELINE; Ser.
No. 09/372,137, filed Aug. 20,1999 entitled APPARATUS AND METHOD FOR FRAGMENT
OPERATIONS IN A 3D GRAPHICS PIPELINE; and Ser. No. 09/378,637, filed Aug. 20,
1999, entitled DEFERRED SHADING GRAPHICS PIPELINE PROCESSOR.

INT-CL: [7] G06T011/40
US-CL-ISSUED: 345/552,345/568 ,345/428 ,345/582 ,345/587
US-CL-CURRENT: 345/552,345/428 ,345/568 ,345/582 ,345/587
FIELD-OF-SEARCH: 345/430;345/501 ;345/506 ;345/502 ;345/503 ;345/507-509
;345/513 ;345/523 ;345/521 ;345/428 ;345/568 ;345/530 ;345/566 ;345/552
;345/536-538 ;345/531

REF-CITED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
Re36145	March 1999	DeAguiar et al.	345/511
4945500	July 1990	Deering	364/522